

# Wafer Level Processing

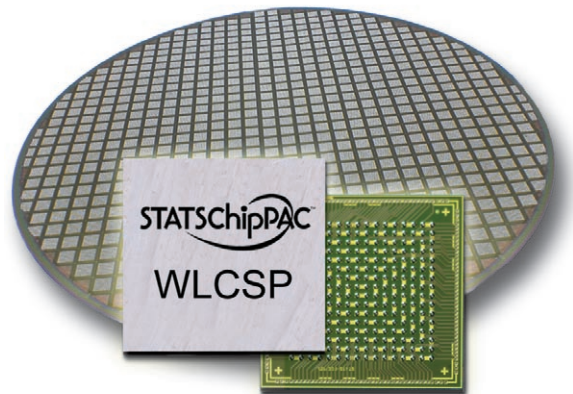
## Wafer Bumping, Wafer Level CSP & Bare Die Processing

### HIGHLIGHTS

- Full service thin film processing, wafer bumping and probing
- Full turnkey wafer bumping and Flip Chip-in-Package assembly capability
- Flexible backend capability for bumped bare die applications

### FEATURES

- In-house thin film on wafer processing and bumping of 200mm and 300mm wafers
- Die services available for 6"-12" wafers (sort, grind, saw and die pick to tape and reel)
- Optional repassivation or redistribution with Polyimide dielectric material
- Redistribution metal options include plated Cu and sputtered AlCu
- Wafer level IPD and thick copper (8-12 $\mu$ m) conductors available
- Bump offering supports STATS ChipPAC's internal Flip Chip-in-Package product offerings, bumped bare die and wafer level chip scale packages (WLCSP) for Flip Chip-on-Board applications
- Bumps formed by printed paste, electroplate or ball drop technologies
- Minimum available flip chip bump pitch of 150 $\mu$ m
- Large bump (250-500 $\mu$ m) processing at 0.40mm pitch and greater for Flip Chip-on-Board and WLCSP applications
- Solder alloys include Eutectic (standard and ultra-low Alpha) as well as Pb-free SAC 405, 305 or 105 (95.5Sn/4.0Ag/0.5Cu, 96.5Sn/3.0Ag/0.5Cu or 98.5Sn/1.0Ag/0.5Cu)
- 0.3mm minimum bumped die height; die heights between 0.40 and 0.80mm are common
- Flexible bare die processing capability including wafer thinning, backside coating, laser marking, automated optical inspection and electronic mapping, pre- and/or post-bump wafer probing and die sorting and picking into either tape and reel or waffle pack formats
- Underfilling of substrate mounted bumped die may or may not be required depending on the customer's specific application and reliability requirements
- Underfilling by overmolding is feasible



### DESCRIPTION

STATS ChipPAC's Wafer Level Processing (WLP) services include full service wafer bumping with polyimide dielectric options for wafer repassivation, redistribution and IPD layers. The solder alloy selection can be optimized to the product through the use of a printed paste or ball drop solder bump technology. This internal wafer bumping capability enables full turnkey Flip Chip-in-Package assembly and test. For larger pitch applications, either printed paste bumping or mechanical ball drop are available. Additionally, a complete, flexible backend assembly capability allows for high volume wafer sorting, automatic optical inspection and backend processing into bare die in tape and reel or waffle pack for Flip Chip-on-Board applications by the end user.

### APPLICATIONS

STATS ChipPAC's WLP service enables full service low-end through high-end Flip Chip-in-Package solutions for wireless and portable products as well as high-end networking and computing applications.

The lower end bumped bare die are targeted towards high performance, form factor sensitive, and lower I/O applications primarily within the wireless and handheld product space.

# Wafer Level Processing

## Wafer Bumping, Wafer Level CSP & Bare Die Processing

### SPECIFICATIONS

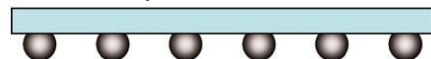
<b>Die Thickness</b>	6" 200-660 $\mu$ m (8-26mils) 8" 200-760 $\mu$ m (8-30mils) 12" 250-790 $\mu$ m (10-31mils)
<b>Bump Pitch Range</b>	150 $\mu$ m minimum
<b>Bump Height</b>	Printed bump -> 70 $\mu$ m Ball drop -> (250 $\mu$ m sphere)
<b>Wafer Thinning</b>	Fully automated backgrinding Et mechanical polishing
<b>Backside Coating</b>	Laminated coating
<b>Marking</b>	Laser marking
<b>Inspection</b>	Automatic optical inspection with electronic wafer mapping
<b>Packing Options</b>	Fully automated die pick/place into custom pocket tape/reel or waffle pack media

### ELECTRICAL PERFORMANCE

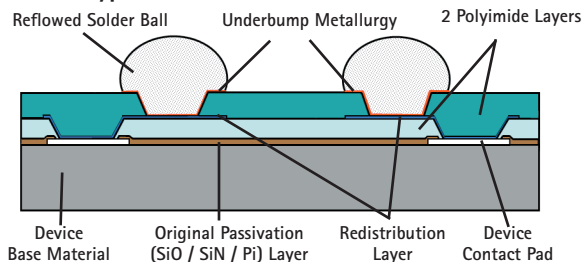
- Dependent on application design, but capable to beyond 10GHz
- Application specific electrical characterization available upon request
- Thick Cu for high current low inductance applications

### CROSS-SECTIONS *(Not to scale)*

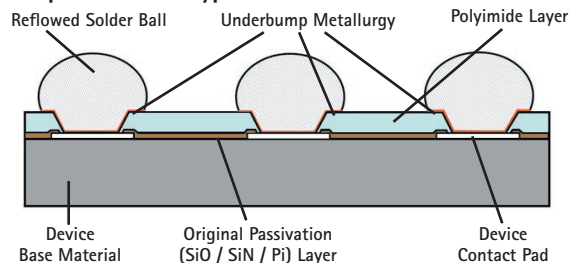
#### WLCSP Bumped Bare Die



#### "RDL" Type WLCSP



#### "Repassivation" Type WLCSP



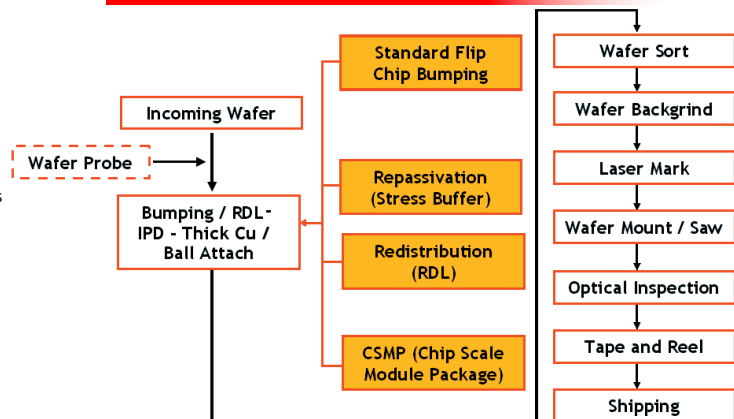
### COMPONENT LEVEL RELIABILITY TESTING

<b>Moisture Sensitivity Level</b>	Eutectic printed bump: JEDEC Level 3 @ 220°C Pb-free printed bump: JEDEC Level 3 @ 260°C
<b>Temperature Cycling</b>	-55°C/125°C, 1000 cycles (eutectic Et Pb-free printed bumps)
<b>High Temperature Storage</b>	150°C, 1000 hrs (eutectic Et Pb-free printed bumps)
<b>Multiple Solder Reflow</b>	5x, 10x and 20x reflows with minimal reduction in bump shear strength
<b>Pressure Cooker Test</b>	121°C/ 100% RH, 168 hrs

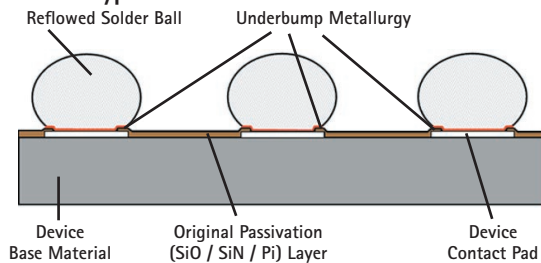
### THERMAL PERFORMANCE

- Thermal performance in the 20-40°C/W range for a 5mm x 5mm die without thermal enhancement
- Application specific thermal characterization available upon request

### GENERIC WLCSP PROCESS FLOW



#### "FOC" Type WLCSP



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