

Flip Chip BGA

fcBGA, fcBGA-SiP, fcBGA-H, fcBGA-MP

HIGHLIGHTS

- High performance packages up to 55mm body size with >2900 pins, and thermal solutions ranging from 2 piece, 1 piece or no heat spreader
- ABF build up to 4-4-4 (5-2-5 in development) and 2L and 4L (1-2-1) laminate substrates with 400 μ m thin core (200 μ m core and coreless in development)
- Packaging solution for 40N node with Ultra low K die-electric (32N/28N in development)
- "Green" flip chip solution with Pb-free, Cu-column bump and halogen-free material sets

FEATURES

- 65N/Low K & 40N/ELK
- Eutectic, High Pb & Pb-free & Cu-column bumps
- Nitride, Polyimide, BCB wafer passivations
- Ni-Au, SOP (solder-on-pad), OSP (organic solder preservative), Ni-free SOP pad & immersion tin finish
- Bumped wafer thinning down to 100 μ m
- Wafer bumping for 200mm (printing) & 300mm (plating) wafers; RDL for 200mm wafers
- Seamless integration of flip chip, SMT & in-line open/short testing operations
- F/A metrology tools for rapid diagnostics & debugging, including TDR, CSAM, X-ray, Ion milling & SEM
- All packages qualified to JEDEC specifications and/or custom requirements based on end applications

APPLICATIONS

- ASIC and FPGAs requiring high pin counts and electrical performance
- CPUs driven by electrical performance
- GPU (Graphics Processing Units) requiring electrical performance & efficient on-chip power distribution
- PC chip sets & integrated graphics devices (IGP) driven by high I/O density



DESCRIPTION

STATS ChipPAC's high-end BGA Flip Chip packages include the fcBGA, fcBGA-SiP, fcBGA-H and fcBGA-MP. The fcBGA package is the main platform in this package sub-group, which also includes a thermally enhanced version with heat spreader (fcBGA-H) and a package subsystem meeting the standard BGA footprint that contains multiple components within the same package (fcBGA-MP).

STATS ChipPAC's Flip Chip BGA packages are available in ball counts ranging from 32 to 2915, body sizes from 5 x 5mm to 55 x 55mm and various package formats.

Flip Chip interconnection provides the ultimate in miniaturization, reduced package parasitics and enables new paradigms in the area of power and ground distribution to the chip which are not feasible with other traditional packaging approaches. STATS ChipPAC offers full turnkey services ranging from design through production, including high speed, high pin count digital and RF testing.

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SPECIFICATIONS

Die Thickness	6" 150-660 μ m (6-26mils) 8" 150-760 μ m (6-30mils) 12" 150-787 μ m (6-31mils)
Bump Pitch	150 μ m area array
Marking	Ink or laser
Packing Options	JEDEC tray

RELIABILITY

Moisture Sensitivity Level	JEDEC Level 4 or 3 (peak temp 230°, 245° or 260°)
Temperature Cycling	-55°C/125°C, 1000 cycles (typical)
High Temperature Storage	150°C, 1000 hrs (typical)
Unbiased HAST	130°C, 85% RH, 2 atm, 96 hrs (typical)

THERMAL PERFORMANCE

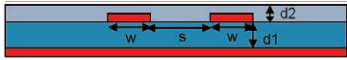
Body Size (mm)	Ball Count	Die Size (mm)	θ_{jc} (°C/W)	Natural Convection	θ_{ja} (°C/W) 1 m/s	2 m/s
31	792	9.6	1.1	14.0 / 10.0*	11.8 / 6.0*	11.0 / 5.7*
35	964	11.1	0.8	12.5 / 8.9*	11.0 / 5.5*	10.0 / 5.2*
40	1161	12.8	0.6	11.2 / 8.0*	9.4 / 4.8*	8.4 / 4.4*
40	1417	15.1	0.4	10.7 / 7.6*	8.7 / 4.3*	7.7 / 4.0*
45	1732	17.4	0.3	9.0 / 6.5*	7.5 / 3.9*	6.5 / 3.5*

Notes: *Includes heat sink (0.5" tall, channel design). Simulation data for package mounted on 4 layer PCB (per JEDEC JESD51-9) under natural convection as defined in JESD51-2.

ELECTRICAL PERFORMANCE

Parametric Data: Sample Embedded Micro-Stripline Configuration

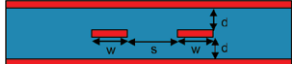
Metal Thickness	Prepreg Thickness(d1)	Solder Mask Thickness(d2)	Trace Width(w)	Trace Spacing(s)	Inductance (nH/mm)	Capacitance (pF/mm)	Ind. Trace Lossy Z11@1GHz	Diff. Pair Lossy Zdiff@1GHz	Lossy Propagation Delay Even Mode	Lossy Propagation Delay Odd Mode
15 μ m	40 μ m	35 μ m	25 μ m	25 μ m	0.408	0.109	69.9 Ω	84.1 Ω	6.10ps/mm	6.54ps/mm
				40 μ m	0.414	0.097	70.9 Ω	100.4 Ω	6.12ps/mm	6.39ps/mm



Conductor material = copper
Prepreg material dielectric constant = 3.4@1GHz
Solder mask material dielectric constant = 3.9@1GHz

Parametric Data: Sample Stripline Configuration

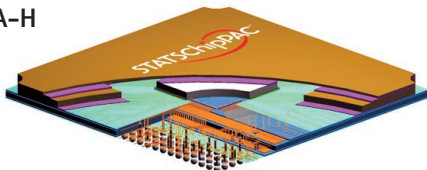
Metal Thickness	Prepreg Thickness(d)	Trace Width(w)	Trace Spacing(s)	Inductance (nH/mm)	Capacitance (pF/mm)	Ind. Trace Lossy Z11@1GHz	Diff. Pair Lossy Zdiff@1GHz	Lossy Propagation Delay Even Mode	Lossy Propagation Delay Odd Mode
15 μ m	40 μ m	25 μ m	25 μ m	0.323	0.126	54.6 Ω	81.6 Ω	6.37ps/mm	6.46ps/mm
			50 μ m	0.329	0.117	55.5 Ω	99.0 Ω	6.38ps/mm	6.40ps/mm



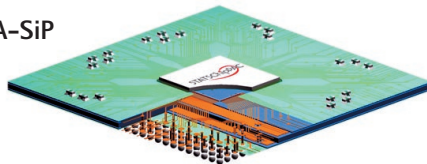
Conductor material = copper
Prepreg material dielectric constant = 3.4@1GHz
Solder mask material dielectric constant = 3.9@1GHz

CROSS-SECTIONS

fcBGA-H



fcBGA-SiP



PACKAGE CONFIGURATIONS

Package Size (mm)	Lead Count	Bump Pitch (μ m)	Bump Count	Substrate	Layer
12	160	200	-	Laminate	2L
14	493	187	716	B/U	4L
15	169	194	153	Laminate	2L
23	548	180	726	B/U	6L
29	969	170	1129	B/U	6L
31	701	225	1271	B/U	8L
	736	340	976	Laminate	4L
	899	150	2796	B/U	6L
35	956	225	2700	B/U	6L
	960	340	1935	Laminate	4L
	960	225	2703	B/U	6L, 8L
	1017	160	3284	B/U	8L
40	1156	150	5590	B/U	8L
	1004	250	2116	B/U	8L
	1012	225	3138	B/U	8L
	1157	240	1876	Laminate	4L
	1413	225	3599	B/U	8L, 5L
42.5	1677	225	4488	B/U	8L
45	1728	225	4899	B/U	8L
55	2915	180	7550	B/U	12L

Corporate Office 10 Ang Mo Kio St. 65, #05-17/20 Techpoint, Singapore 569059 Tel: 65-6824-7777 Fax: 65-6720-7823

Global Offices USA 510-979-8000 JAPAN 81-03-3507-5675 CHINA 86-21-5976-5858 MALAYSIA 603-4257-6222
KOREA 82-31-639-8911 TAIWAN 886-3-593-6565 UK 44-1483-413-700 NETHERLANDS 31-38-333-2023